AMENDMENTS TO THE CLAIMS:

Complete Listing of Claims

Claims 1-4 (canceled)

Claim 5. (currently amended) A method of testing a serial transceiver chip for jitter tolerance, the transceiver including at least one transmitter and at least one receiver, the method comprising:

generating a serialization clock;

adding one or more known and controlled amount of jitter to the serialization clock;

transmitting a known sequence of test signals using the serialization clock with the added jitter;

causing a clock and data recovery mechanism in a receiver to recover the test signals; and

comparing the recovered test signals with said known sequence of test signals thereby testing the ability of the clock and data recovery mechanism to tolerate the jitter that was added;

wherein the steps of generating a serialization clock, adding one or more known and controlled amount of jitter to the serialization clock, transmitting a known sequence of test signals using the serialization clock with the added jitter, and causing a clock and data recovery mechanism in the receiver to recover the test signals with jitter are all performed inside the serial transceiver chip, and ~~The method of claim 1~~ wherein adding one or more known and controlled amount of jitter is performed by use of an interpolator

and an interpolator control mechanism programmed to create the known and controlled amount of jitter.

Claim 6. (original) The method of claim 5 wherein the known sequence of test signals is created by a PRBS (Pseudo Random Binary Sequence) generation mechanism and wherein comparing the recovered test signals is done by use of the PRBS verification mechanism.

Claim 7. (original) The method of claim 6 wherein creating the known sequence of test signals and comparing the recovered sequence of test signals is performed inside the serial transceiver chip.

Claim 8. (original) The method of claim 5 wherein the known sequence of test signals is created inside the serial transceiver chip and wherein comparing the recovered sequence of test signals is also performed inside the serial transceiver chip.

Claims 9-12 (canceled)

Claim 13. (currently amended) A method of testing a serial receiver for jitter tolerance, the serial receiver being fully contained on a single semiconductor substrate, the method comprising:

generating a known sequence of test signals containing negligible jitter relative to a local reference clock;

causing a clock and data recovery mechanism in the serial receiver to recover the test signals;

adding one or more known and controlled amount of jitter into the clock recovery mechanism to force the clock recovery mechanism to compensate for the added jitter; and

comparing the recovered test signals with said known sequence of test signals thereby testing the ability of the clock and data recovery mechanism to tolerate the jitter that was added;

wherein the steps of causing a clock and data recovery mechanism in the receiver to recover the test signals, and adding the known and controlled amount of jitter to the clock recovery mechanism are all performed inside the serial receiver

The method of claim 9 wherein adding one or more known and controlled amount of jitter is performed by use of an interpolator control mechanism programmed to create the known and controlled amount of jitter.

Claim 14. (original) The method of claim 13 wherein the known sequence of test signals is created by a PRBS (Pseudo Random Binary Sequence) generation mechanism and wherein comparing the recovered test signals is done by use of a PRBS verification mechanism.

Claim 15. (original) The method of claim 14 wherein comparing the recovered sequence of test signals is performed inside the serial receiver.

Claim 16. (original) The method of claim 13 wherein comparing the recovered sequence of test signals is performed inside the serial receiver.

Claim 17 (canceled)

Claim 18. (currently amended) A method of testing a serial transceiver for jitter transfer, the serial transceiver including at least one transmitter and at least one receiver, the serial transceiver being fully contained on a single semiconductor substrate, the method comprising:

generating a serialization clock;

adding one or more known and controlled amounts of jitter to the serialization clock;

transmitting a sequence of test signals using the serialization clock with the added jitter;

causing a clock and data recovery mechanism in a receiver to recover a clock signal from the transmitted sequence of test signals;

monitoring and measuring an amount of jitter present in the recovered clock signal; and

comparing jitter present in the recovered clock with jitter added to the serialization clock thereby testing the jitter transfer characteristic of the transceiver;

wherein the steps of generating a serialization clock, adding jitter to the serialization clock, transmitting a sequence of test signals, monitoring and measuring an amount of jitter in the recovered clock signal, and comparing jitter present in the recovered clock with jitter added to the serialization clock are all performed inside the serial transceiver, and ~~The method of claim 17~~ wherein adding one or more known and controlled amounts of jitter is performed by use of an interpolator and an interpolator control mechanism programmed to create the known and controlled amounts of jitter.

Claim 19. (currently amended) A method of testing a serial transceiver for jitter transfer, the serial transceiver including at least one transmitter and at least one receiver, the serial transceiver being fully contained on a single semiconductor substrate, the method comprising:

generating a serialization clock;

adding one or more known and controlled amounts of jitter to the serialization clock;

transmitting a sequence of test signals using the serialization clock with the added jitter;

causing a clock and data recovery mechanism in a receiver to recover a clock signal from the transmitted sequence of test signals;

monitoring and measuring an amount of jitter present in the recovered clock signal; and

comparing jitter present in the recovered clock with jitter added to the serialization clock thereby testing the jitter transfer characteristic of the transceiver;

wherein the steps of generating a serialization clock, adding jitter to the serialization clock, transmitting a sequence of test signals, monitoring and measuring an amount of jitter in the recovered clock signal, and comparing jitter present in the recovered clock with jitter added to the serialization clock are all performed inside the serial transceiver, and ~~The method of claim 17~~ wherein monitoring and measuring the amount of jitter present in the recovered clock signal is performed by use of an up/down counter that is responsive to direction and step control signals for an interpolator used for clock recovery, and wherein comparing the jitter present in the recovered clock

signal is performed by use of a programmable comparator set to issue a warning if a maximum count achieved by an up/down counter exceeds the maximum allowed to pass the transfer test.

Claim 20. (currently amended) A method of testing a serial transceiver for jitter transfer, the serial transceiver including at least one transmitter and at least one receiver, the serial transceiver being fully contained on a single semiconductor substrate, the method comprising:

generating a serialization clock;

adding one or more known and controlled amounts of jitter to the serialization clock;

transmitting a sequence of test signals using the serialization clock with the added jitter;

causing a clock and data recovery mechanism in a receiver to recover a clock signal from the transmitted sequence of test signals;

monitoring and measuring an amount of jitter present in the recovered clock signal; and

comparing jitter present in the recovered clock with jitter added to the serialization clock thereby testing the jitter transfer characteristic of the transceiver;

wherein the steps of generating a serialization clock, adding jitter to the serialization clock, transmitting a sequence of test signals, monitoring and measuring an amount of jitter in the recovered clock signal, and comparing jitter present in the recovered clock with jitter added to the serialization clock are all performed inside the serial transceiver, and ~~The method of claim 17~~ wherein:

adding one or more known and controlled amounts of jitter is performed by use of an interpolator and an interpolator control mechanism programmed to create the known and controlled amounts of jitter;

monitoring and measuring the amount of jitter present in the recovered clock signal is performed by use of an up/down counter that is responsive to direction and step control signals for the interpolator used for clock recovery;

comparing jitter present in the recovered clock with jitter added to the serialization clock is performed by use of a programmable comparator that is set to issue a warning if a maximum count achieved by an up/down counter exceeds a maximum allowed to pass a transfer test.

Claim 21. (original) The method of claim 20 wherein the sequence of test signals are generated on the single semiconductor substrate that also contains the transceiver.

Claims 22, 23 (canceled)

Claim 24. (currently amended) A method of testing a serial receiver for jitter transfer, the serial receiver being fully contained on a single semiconductor substrate, the method comprising:

generating a sequence of test signals containing negligible jitter relative to a local reference clock;

causing a clock recovery mechanism in the serial receiver to recover a clock signal from the sequence of test signals, the clock recovery mechanism contained on the single semiconductor substrate;

adding one or more known and controlled amounts of jitter into the clock recovery mechanism to force the clock recovery mechanism to compensate for added jitter;

monitoring and measuring an amount of activity in the clock recovery mechanism; and

comparing the amount of activity in the clock recovery mechanism with an expected amount of activity that is based on the jitter added thereby testing a jitter transfer characteristic of the receiver;

wherein the steps of adding one or more known and controlled amounts of jitter into the clock recovery mechanism, monitoring and measuring an amount of activity in the clock recovery mechanism, and comparing the amount of activity in the clock recovery mechanism with an expected amount of activity are all performed inside the serial receiver, and ~~The method of claim 23~~ wherein adding one or more known and controlled amounts of jitter is performed by use of an interpolator control mechanism that is programmed to create the known and controlled amounts of jitter.

Claim 25. (original) The method of claim 24 wherein monitoring and measuring the amount of activity in the clock recovery mechanism is performed by use of an up/down counter that is responsive to direction and step control signals for an interpolator used for clock recovery, and wherein comparing the amount of activity in the clock recovery mechanism with the expected amount of activity is performed by use of a programmable comparator set to issue a warning if a maximum count achieved by an up/down counter exceeds the maximum allowed to pass the transfer test.

Claim 26. (currently amended) A method of testing a serial receiver for jitter transfer, the serial receiver being fully contained on a single semiconductor substrate, the method comprising:

generating a sequence of test signals containing negligible jitter relative to a local reference clock;

causing a clock recovery mechanism in the serial receiver to recover a clock signal from the sequence of test signals, the clock recovery mechanism contained on the single semiconductor substrate;

adding one or more known and controlled amounts of jitter into the clock recovery mechanism to force the clock recovery mechanism to compensate for added jitter;

monitoring and measuring an amount of activity in the clock recovery mechanism; and

comparing the amount of activity in the clock recovery mechanism with an expected amount of activity that is based on the jitter added thereby testing a jitter transfer characteristic of the receiver;

wherein the steps of adding one or more known and controlled amounts of jitter into the clock recovery mechanism, monitoring and measuring an amount of activity in the clock recovery mechanism, and comparing the amount of activity in the clock recovery mechanism with an expected amount of activity are all performed inside the serial receiver, and ~~The method of claim 23~~ wherein monitoring and measuring the amount of activity in the clock recovery mechanism is performed by use of an up/down counter that is responsive to direction and step control signals for an interpolator used

for clock recovery, and wherein comparing the amount of activity in the clock recovery mechanism with the expected amount of activity is performed by use of a programmable comparator set to issue a warning if a maximum count achieved by an up/down counter exceeds the maximum allowed to pass the transfer test.

Claim 27. (original) The method of claim 26 wherein the sequence of test signals are generated on the single semiconductor substrate that also contains the receiver.

Claims 28-31 (canceled)

Claim 32. (currently amended) A method of testing a FIFO (First In First Out) circuit on a single semiconductor substrate, the method comprising:

generating an on-chip clock at the same frequency as a reference clock;

incrementally adding a known and controlled amount of phase shifts to the on-chip clock signal;

using the reference clock and the phase-shifted on-chip clock to drive the FIFO circuit; and

measuring an amount of phase-shift that can be added to the on-chip clock signal before the FIFO experiences overflow and/or underflow errors;

wherein the steps of generating an on-chip clock, incrementally adding a known and controlled amount of phase shifts, using the reference clock and the phase-shifted on-chip clock to drive the FIFO circuit, and measuring an amount of phase-shift are all performed on the single semiconductor substrate, and ~~The method of claim 29~~ wherein incrementally adding a known and controlled amount of phase shifts is performed by use of an interpolator and an interpolator control mechanism programmed to create desired phase shifts.

Claim 33. (original) The method of claim 32 and further comprising:

providing a PRBS pattern to be used as input data for the FIFO; and

checking output data from the FIFO with a PRBS verifier, the PRBS verifier being disposed on the single semiconductor substrate.

Claim 34. (original) The method of claim 33 wherein the PRBS pattern is provided by an on-chip PRBS generator clocked by the reference clock signal.

Claims 35-42 (canceled)

Claim 43. (original) An apparatus for inserting known and controlled amount of jitter onto a switching signal, the apparatus comprising:

an interpolator for inserting the jitter; and

an interpolator control mechanism programmed to create the desired jitter.